WHAT IS CLAIMED IS:

1. A semiconductor device provided with a semiconductor circuit having a channel layer over a semiconductor substrate, with an insulation layer lying therebetween, and including a field effect transistor in said channel layer, comprising:

a first insulation layer and a second insulation layer provided between said channel layer and said semiconductor substrate to constitute said insulation layer; and

a potential interconnection layer provided between said first insulation layer and said second insulation layer,

wherein said potential interconnection layer includes a power supply potential region and a ground potential region which are alternately provided, with an interlayer insulation layer lying therebetween, when viewed from a plane, and

selected power supply potential region and ground potential region are each electrically connected to said field effect transistor selected.

2. The semiconductor device according to claim 1, wherein said potential interconnection layer is provided so as to directly contact said first insulation layer and said second insulation layer.

3. The semiconductor device according to claim 1, wherein

said potential interconnection layer includes a first potential interconnection layer provided over said first insulation layer, and a second potential interconnection layer provided over said first potential interconnection layer,

a dielectric layer is provided between said first potential interconnection layer and said second potential interconnection layer,

said first potential interconnection layer is provided with one of said power supply potential region and said ground potential region, and said second potential interconnection layer is provided with the other of said power supply potential region and said ground potential region, and

said power supply potential region and said ground potential region are alternately provided when viewed from a plane.

4. The semiconductor device according to claim 1, wherein

said potential interconnection layer includes a first potential interconnection layer provided over said first insulation layer, and a second potential interconnection layer provided over said first potential interconnection layer,

a dielectric layer is provided between said first potential interconnection layer and said second potential interconnection layer,

said first potential interconnection layer and said second potential interconnection layer are each provided with said power supply potential region and said ground potential region which are alternately provided, with the interlayer insulation layer lying therebetween, when viewed from a plane, and

an extending direction of said power supply potential region and said ground potential region provided in said first potential interconnection layer and an extending direction of said power supply potential region and said ground potential region provided in said second potential interconnection layer are provided so as to cross each other.

5. The semiconductor device according to claim 1, further comprising between said channel layer and said second insulation layer:

a power source layer provided over said second insulation layer; and

a third insulation layer provided over said power source layer,

wherein a body region provided in said channel layer and including a channel region of said field effect transistor connects with said power source layer.